GENERAL REMARKS

Applicant respectfully submits that rejection of claims 14, 16 under 35 U.S.C. 102(b), by Office Action (OA) mailed on 03/22/2005, as being anticipated by Arimoto (6,333,889) is not warranted because this prior art document does not teach all elements of claims 14 and 16.



PAGE 3/7 * RCVD AT 5/4/2005 10:11:19 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:4018851046 * DURATION (mm-ss):01-56

DETAILED REMARKS

The OA states: "Claims 14, 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Arimoto (6,333,889). Regarding to claims 14, 16, Arimoto discloses a wide bandwidth DRAM memory comprising: simultaneously operable connection path between a string of memory cells and corresponding input/output terminals (2), wherein the string of memory cells are essentially all the memory cells which are attached to the same word line, wherein the DRAM memory has a plurality of word lines (WL) and a plurality of memory cells; and a single ended data line structure. See Figs. 1, 12, 16-17; Cols. 8-9, 17, 20-22."

Before discussing Arimoto (6,333,889) ("Arimoto") applicant would like to reiterate the elements of independent claim 14 of the present invention. Claim 14 has the following elements: "string of memory cells" with simultaneous connections to I/O terminals; the memory cells in the string are essentially all the memory cells which are attached to the same wordline; and, the connections from/to the string of memory cells to/from the I/O terminals form a single ended data line structure. Applicant respectfully suggests that Arimoto does not anticipate a fully single ended data line structure, nor anticipates simultaneous read/write connection to essentially all of the cells attached to the same wordline.

First, applicant discusses the data line structure teachings of Arimoto. In general, in large memories the cells are organized into multiple arrays within the whole of the memory, just as Arimoto and also the present invention does. (MA0, ..1, ..2; MB0, ..1, ..2; etc. in Arimoto.) With the subdivision of memory cells into arrays, everything becomes divided into "local", namely dealing with, belonging to an array, and "global", belonging to multiples of arrays and/or to the whole memory. Arimoto in his third and fifth embodiment, Figs. 11, 12, 16, 17, does indeed introduce single ended bitlines, but only globally, between arrays, inside the arrays, locally, the bitline pair structure is maintained. This is most clear in Fig. 11 where Arimoto displays how he accomplishes the transition from bitline pairs (BLP) inside the array, to a single ended internal data line (IOL) between arrays. For both Figs. 12 and 17, the ones where Arimoto shows single ended lines, the specification states that the remaining (not displayed) structure of the memory, including the bitline pair structure inside the arrays, is that of Fig. 1. To quote: "The remaining structure is identical to that of FIG. 1, and corresponding components have the same reference characters allotted." In Col 17, lines 20 -22; and in



PAGE 4/7 * RCVD AT 5/4/2005 10:11:19 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:4018851046 * DURATION (mm-ss):01-56

Col 21, lines 26 - 29: "sub arrays MAB0, MAB1, MAB2 and MAB3 have an internal data line structure identical to that shown in FIG. 1. In each of memory sub arrays MAB0-MAB3, one internal data line pair IOP is arranged per four sense amplifier circuits with respect to one sense amplifier band." (Again. IOP is bitline pair sturcture inside the arrays.) That is, to emphasize again, inside the arrays Arimoto always, in all the embodiments, uses paired bitline structure. In contrast, the present invention has, and claims, "a single ended data line structure" meaning all the way between cells and I/Os, completely free of bitline pairs even inside the arrays. To accomplish this, the invention also presents and teaches single ended sensing, see for instance Fig. 2A. In fact, for the memory of the invention the full single ended bitline structure (even inside the arrays) is essential as stated for instance on page 11 lines 9 -12: "Without the single ended global bitline structure the width of the data-bus would be limited by the metal wire pitch availability in laying out the data-lines in the DRAM array. The small global bitline voltage scheme is used in conjunction with the single ended data-line structure to achieve wide I/O, high bandwidth, and low power." Accordingly, applicant respectfully avers, that since Arimoto uses bit line pairs inside the arrays, this prior art document does not anticipate a complete memory with a single ended data line structure.

Applicant would like to turn now to the question of whether Arimoto teaches the read/write of essentially all of the cells attached to the same wordline. In relating to the fifth embodiment, Col. 20 lines 54 - 57 in Arimoto states: "More specifically, the number of data bits that can be transferred at one time can be made equal to the number of memory cells connected to one word line WL. Therefore, the data transfer rate can be improved significantly." However, this statement simply avers that the number of bits transferred equals the number of cells connected to one wordline, it does not say that these bits indeed come only from such cells that are connected to the same wordline. And indeed, reading the specification makes it clear that Arimoto never reads/writes, or in general transfers bits involving all the cells attached to the same single wordline. Arimoto achieves the transfer rate of bits equaling the number of cells connected to a wordline by transferring bits from several differing arrays (MAB0, MAB1, ..), in each case involving only a fraction, such as N/2 or N/4, of the cells that are attached to any given wordline. In each and every embodiment, from one to seven, Arimoto discusses in detail, and shows in the figures (CW.., CD.., CG.. in general with symbols starting with the letter "C"), how the column select , lines, amplifiers, signals, etc. are being handled. Column select is the



PAGE 5/7 * RCVD AT 5/4/2005 10:11:19 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:4018851046 * DURATION (mm-ss):01-56

operation, and hardware, which selects out from all the cells attached to the same wordline, the fraction which is involved in a simultaneous transfer operation. Arimoto usually transfers 1/4 or 1/2 of such cells, as is discussed throughout the specification. For instance, when the transfer rate is "equal to the number of memory cells connected to one word line" which is the case of the quote from Col 21 as above, Arimoto transfers bits form four arrays (MAB0 to MAB3) simultaneously, involving 1/4-th of the cells from each. (For completeness applicant remarks, that the bitline pair structure inside the arrays, and the need for column selection are connected. Arimoto cannot transfer bits involving all the cells attached to the same wordline because the bitline pair structure inside the arrays does not give Arimoto sufficient wire density to reach simultaneously all of the cells.) In contrast, the present invention does not contain column selection, as not needed because all of the cells (without having to select any in particular) which are attached to the same wordline are always transferring bits simultaneously. Thus, applicant respectfully contends that Arimoto does not have, does not teach, and does not anticipate full wordline width transfer, namely involving in transfer "all the memory cells which are attached to the same wordline".

In view of the preceding discussion, applicant respectfully contends that claim 14 in view of Arimoto is novel and patentable. Furthermore, claim 16 depending on claim 14, and including further limitations, is a fortiori patentable.

Additional prior art made of record, US patent 6,075,741 to Ma et al., teaches gradual power up of circuits, and does not anticipate or renders obvious the present invention.

Applicant cancels all of the APPENDIX, pages A1 to A12, which contained detailed numerical simulations on the functioning of circuits of the invention, and which APPENDIX was submitted together with the application on 08/06/2003.

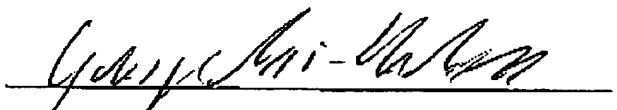


PAGE 6/7 * RCVD AT 5/4/2005 10:11:19 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:4018851046 * DURATION (mm-ss):01-56

CLOSING STATEMENTS

On the basis of the above remarks applicant respectfully submits that claims 14 and 16 are patentable, and that this application is in condition for allowance, which action is respectfully requested.

Respectfully,



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PAGE 7/7 * RCVD AT 5/4/2005 10:11:19 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/0 * DNIS:8729306 * CSID:4018851046 * DURATION (mm-ss):01-56